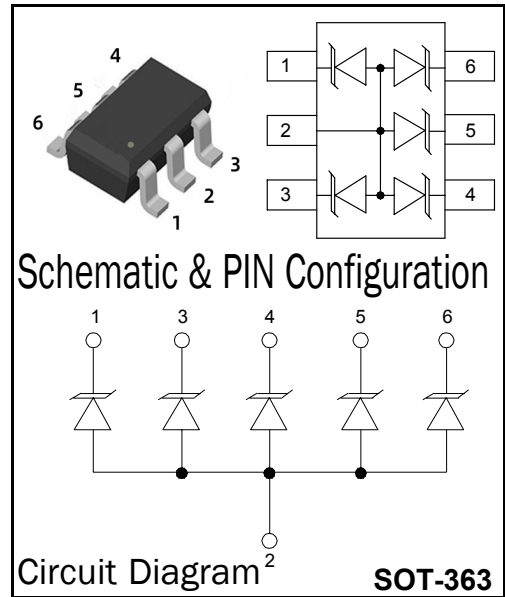


Tvs Diode Array For ESD and Latch-Up Protection
Features

- ◆ESD protection for data lines to IEC 61000-4-2(ESD)+15kV(air), ± 8kV(contact)
- IEC61000-4-4(EFT) 40A (5/50ns)
- ◆Small package for use in portable electronics
- ◆Protects five I/o lines
- ◆Working voltage: 5V
- ◆Low leakage current
- ◆Low operating and clamping voltages
- ◆Solid-state silicon-avalanche technology

Application

- ◆Cellular Handsets and Accessories
- ◆Cordless Phones
- ◆Personal Digital Assistants (PDA's)
- ◆Notebooks and Handhelds
- ◆Portable Instrumentation
- ◆Digital Cameras
- ◆Peripherals
- ◆MP3 Players


Marking Code

SMF05C

5C

Absolute Maximum Ratings Ta= 25°C

Symbol	Parameter	Conditions	value	Unit
P _{PK}	Peak Pulse Power	tP = 8/20 μs	100	W
I _{PP}	Peak Pulse Current	tP = 8/20 μs	8	A
V _{ESD}	ESD per IEC 61000-4-2 ESD per IEC 61000-4-2	Air Contact	20 15	KV
T _L	Lead Soldering Temperature	-	260(10seconds)	V
T _J	Operating Temperature	-	-55 to+125	°C
T _{stg}	Storage Temperature Range	-	-55 to+150	°C

Electrical Characteristics Ta = 25°C

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
V _{RWM}	Reverse Stand-Off Voltage		-	-	5	V
V _{BR}	Reverse Breakdown Voltage	I _T = 1mA	6	-	-	V
I _R	Reverse Leakage Current	V _{RWM} = 36 V; T = 25 °C	-	-	5	uA
V _C	Clamping Voltage	I _{PP} =5 A, tP =8/20μs	-	-	9.8	V
V _C	Clamping Voltage	I _{PP} =8 A, tP =8/20μs	-	-	12.5	V
C _J	Junction Capacitance	V _R = 0V, f = 1 MHz	-	-	130	pF

Typical Characteristics

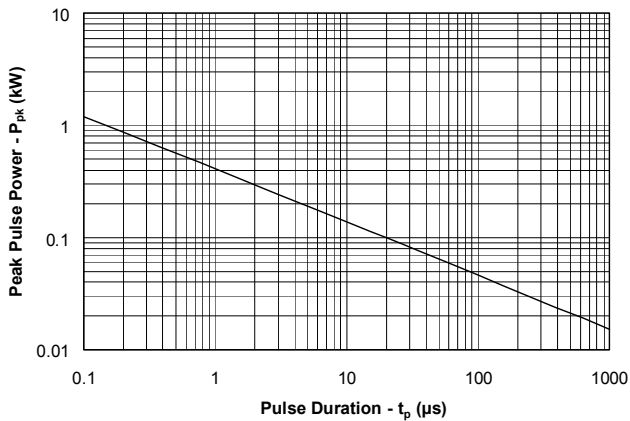


Fig.1 Non-Repetitive Peak Pulse Power vs. Pulse Time

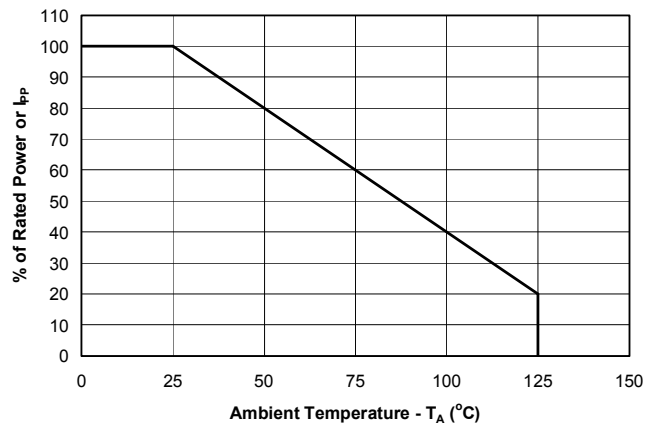


Fig.2 Power Derating Curve

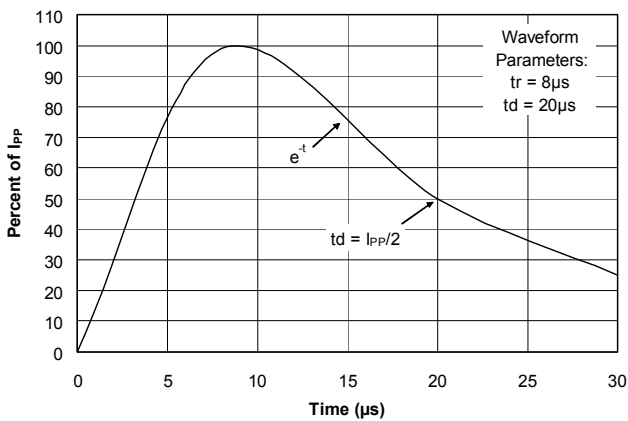


Fig.3 Pulse Waveform

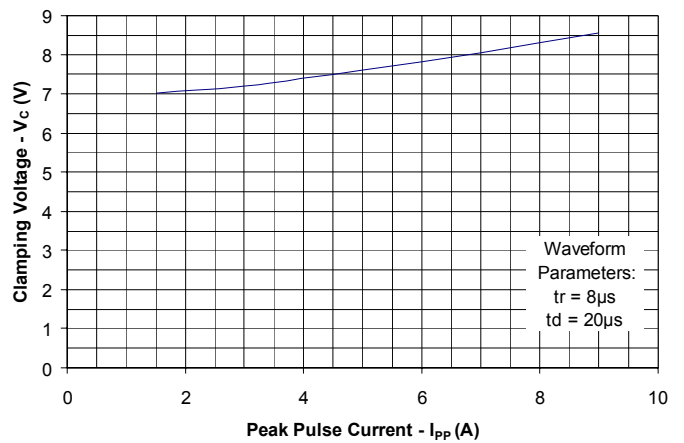


Fig. 4 Clamping Voltage vs. Peak Pulse Current

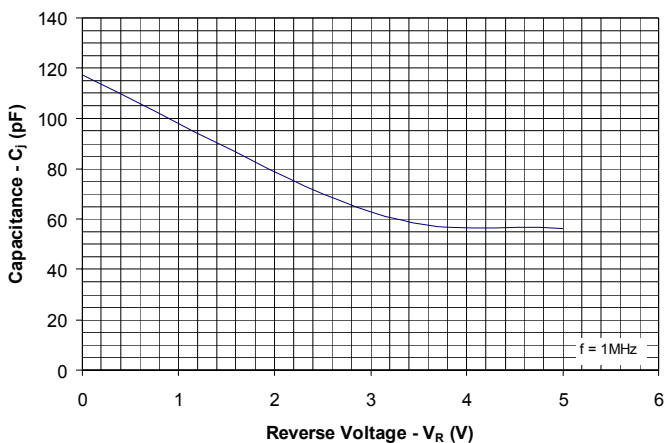


Fig. 5 Capacitance vs. Reverse Voltage

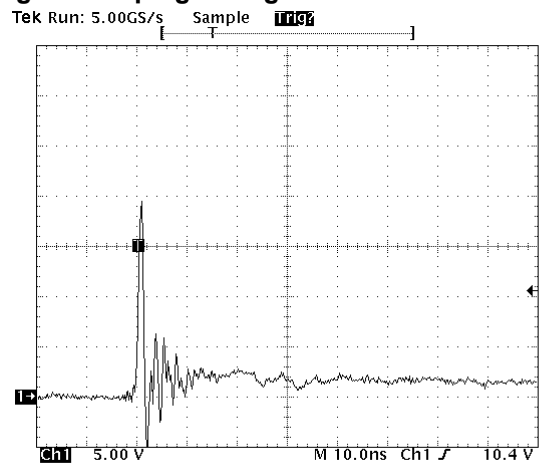


Fig. 6 ESD Clamping Characteristics (8kV Contact Discharge per IEC 61000-4-2)

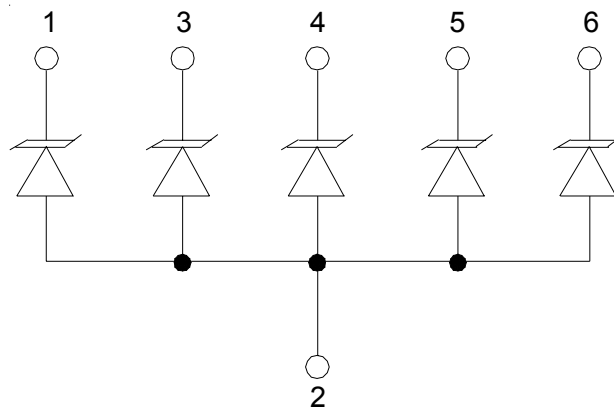
Device Connection for Protection of Five Data Lines

The SMF05C is designed to protect up to five unidirectional data lines.

The device is connected as follows:

- 1, Unidirectional protection of five I/O lines is achieved by connecting pins 1,3, 4,5 and 6 to the data lines.
Pin 2 is connected to ground. The ground connection should be made directly to the ground plane for best results. The path length is kept as short as possible to reduce the effects of parasitic inductance in the board traces.

SMF05C Circuit Diagram

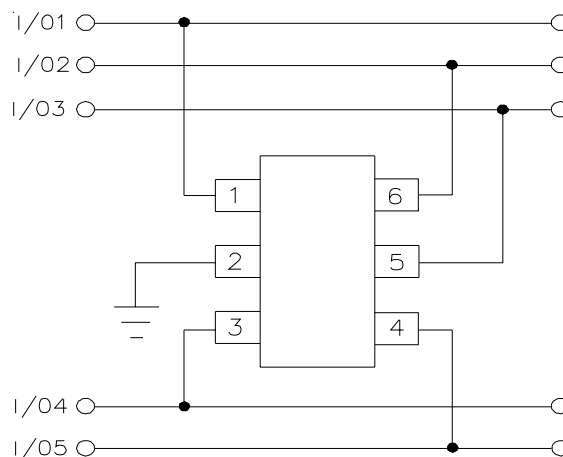


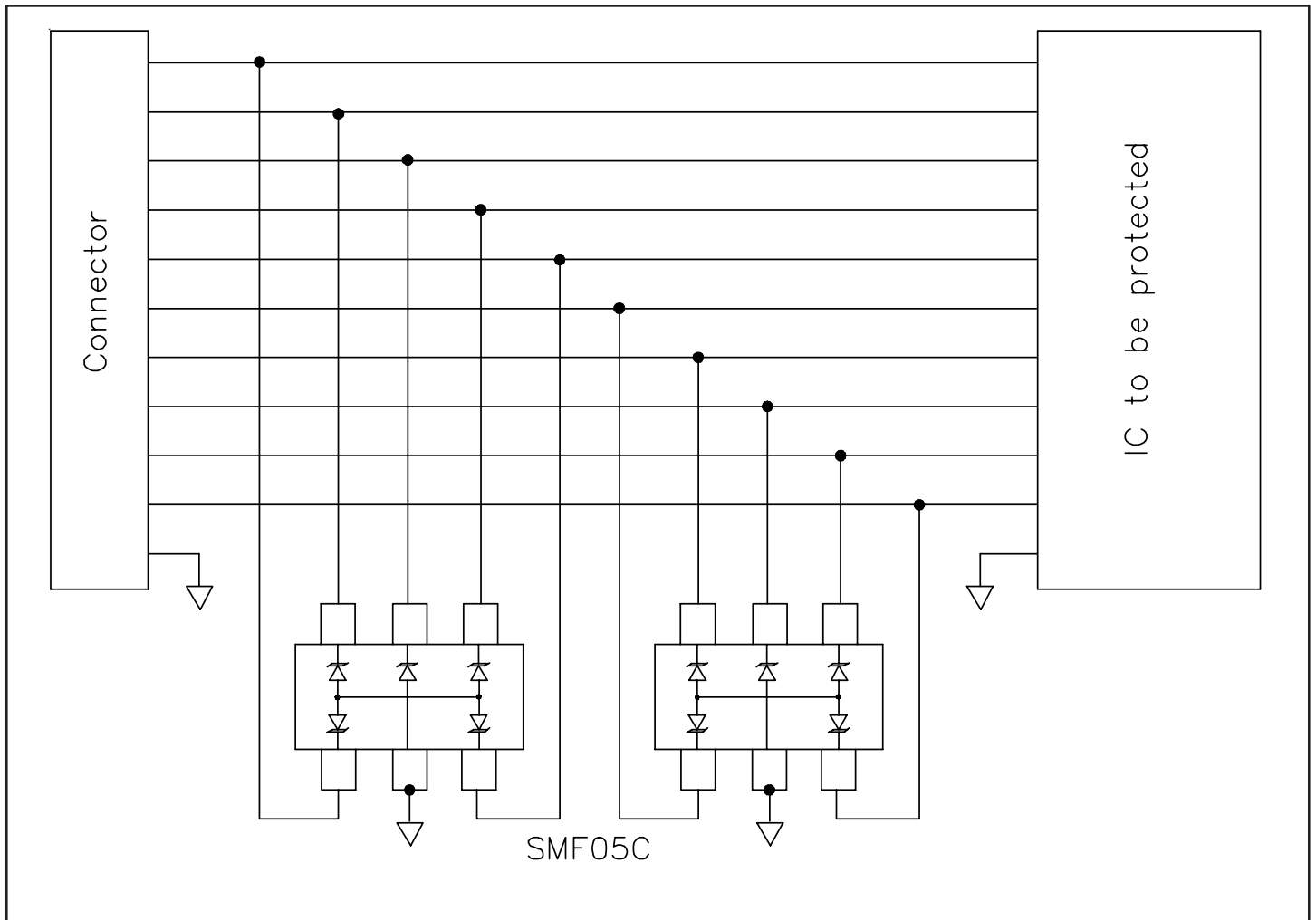
Circuit Board Layout Recommendations for Suppression of ESD.

Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

- 1. Place the SMF05C near the input terminals or connectors to restrict transient coupling.
- 2. Minimize the path length between the SMF05C and the protected line.
- 3. Minimize all conductive loops including power and ground loops.
- 4. The ESD transient return path to ground should be kept as short as possible.
- 5. Never run critical signals near board edges.
- 6. Use ground planes whenever possible.

Protection of Five Unidirectional Lines





Ordering information

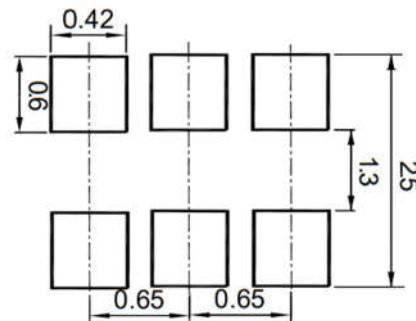
Package	Packing Description	Packing Quantity
SOT-363	Tape/Reel,7"reel	3000PCS/Reel 120000PCS/Carton

Package Dimensions

SOT-363

Dim.	Millimeter(mm)		mil	
	Min.	Max.	Min.	Max.
A	0.8	1.1	32	43
A1	-	0.1	-	3.94
bp	0.20	0.30	7.87	11.81
c	0.10	0.25	3.94	9.84
D	1.8	2.2	70.87	86.61
E	1.15	1.35	45.28	53.15
e	1.3		51.18	
e1	0.65		25.6	
HE	2.0	2.2	78.74	86.6
Lp	0.15	0.45	5.90	17.71
Q	0.15	0.25	5.90	9.84
v	0.2		7.78	
w	0.2		7.78	
y	0.1		3.94	

The recommended mounting pad size



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